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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/779,424	02/08/2001	Paras A. Shah	COMP:0187/FLE (P00-3008)	5601

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INTELLECTUAL PROPERTY ADMINISTRATION
LEGAL DEPARTMENT, M/S 35
P.O. BOX 272400
FT. COLLINS, CO 80527

EXAMINER	
KNOLL, CLIFFORD H	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 10/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/779,424	SHAH, PARAS A.	
	Examiner	Art Unit	
	Clifford H Knoll	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is responsive to communication filed 7/22/04. Currently claims 1-30 are pending.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

Claims 1-15 and 22-30 are rejected under 35 U.S.C. 102(e) as being anticipated by MacLaren (US 6108741).

Regarding claims 1, 6, 9, and 12, discloses temporarily storing a plurality of transaction entries (e.g., col. 28, lines 34-37), selecting one of the plurality of temporarily stored transaction entries and enqueuing the selected one of the plurality of temporarily stored transaction entries (e.g., col. 29, lines 64-66).

Regarding claims 2, 7, 10, and 13, *MacLaren* also discloses wherein (a) temporarily stores a plurality of transaction entries in a bank of registers (e.g., col. 28, lines 34-37).

Regarding claim 3, *MacLaren* also discloses wherein the plurality of transaction entries is temporarily stored simultaneously (e.g., col. 14, lines 22-23).

Regarding claims 4, 8, 11, and 14 *MacLaren* also discloses determining whether a posted write transaction entry is present; if the posted write transaction entry is present, then enqueuing the posted write transaction entry into the transaction order queue (e.g., col. 26, lines 60-63), if the posted write transaction entry is not present, then determining whether a read completion transaction entry is present; if the read completion transaction entry is present, then enqueuing the read completion transaction entry into the transaction order queue (e.g., col. 29, lines 17-26, though not represented in *MacLaren*'s "TRQ" they are nonetheless enqueued as claimed); if the read completion transaction entry is not present, then determining whether a delayed/split transaction entry is present; and if the delayed/split transaction entry is present, then enqueuing delayed/split transaction entry into the transaction order queue (e.g., col. 29, lines 13-15).

Regarding claims 5 and 15, *MacLaren* also discloses enqueuing each of the plurality of transaction entries into the transaction order queue one at a time during successive clock cycles (e.g., col. 30, lines 30-37).

Regarding claim 22, *MacLaren* discloses one processor and a memory device operatively coupled to the at least one processor (e.g., col. 5, lines 9-12); and a transaction order queue circuit configured to process transactions from the memory device, the transaction order queue circuit being adapted to encode a plurality of simultaneous transaction entries (e.g., col. 14, lines 22-23).

Regarding claim 23, *MacLaren* also discloses determining whether a posted write transaction entry is present; if the posted write transaction entry is

present, then enqueuing the posted write transaction entry into the transaction order queue (e.g., col. 26, lines 60-63), if the posted write transaction entry is not present, then determining whether a read completion transaction entry is present; if the read completion transaction entry is present, then enqueuing the read completion transaction entry into the transaction order queue (e.g., col. 29, lines 17-26, though not represented in *MacLaren*'s "TRQ" they are nonetheless enqueued as claimed); if the read completion transaction entry is not present, then determining whether a delayed/split transaction entry is present; and if the delayed/split transaction entry is present, then enqueuing delayed/split transaction entry into the transaction order queue (e.g., col. 29, lines 13-15).

Regarding claim 24, *MacLaren* also discloses wherein the computer system comprises network capabilities (e.g., col. 67, lines 43-44).

Regarding claim 25, *MacLaren* discloses temporarily storing a plurality of simultaneous transaction entries (e.g., col. 14, lines 22-23); and delivering the plurality of transaction entries to a transaction order queue one at a time (e.g., col. 30, lines 30-37).

Regarding claim 26, *MacLaren* also discloses the plurality of simultaneous transaction entries is stored in a bank of registers (e.g., col. 28, lines 34-37).

Regarding claim 27, *MacLaren* also discloses determining whether a posted write transaction entry is present; if the posted write transaction entry is present, then enqueuing the posted write transaction entry into the transaction order queue (e.g., col. 26, lines 60-63), if the posted write transaction entry is not present, then determining whether a read completion transaction entry is present;

if the read completion transaction entry is present, then enqueuing the read completion transaction entry into the transaction order queue (e.g., col. 29, lines 17-26, though not represented in *MacLaren*'s "TRQ" they are nonetheless enqueued as claimed); if the read completion transaction entry is not present, then determining whether a delayed/split transaction entry is present; and if the delayed/split transaction entry is present, then enqueuing delayed/split transaction entry into the transaction order queue (e.g., col. 29, lines 13-15).

Regarding claim 28, *MacLaren* discloses temporarily storing a plurality of simultaneous transaction entries (e.g., col. 14, lines 22-23); prioritizing each of the temporarily stored transaction entries; transmitting the stored transaction entries to the transaction order queue according to priority (e.g., col. 28, lines 34-44).

Regarding claim 29, *MacLaren* also discloses the plurality of transaction entries is stored simultaneously in a bank of registers (e.g., col. 28, lines 34-37).

Regarding claim 30, *MacLaren* also discloses determining whether a posted write transaction entry is present; if the posted write transaction entry is present, then enqueuing the posted write transaction entry into the transaction order queue (e.g., col. 26, lines 60-63), if the posted write transaction entry is not present, then determining whether a read completion transaction entry is present; if the read completion transaction entry is present, then enqueuing the read completion transaction entry into the transaction order queue (e.g., col. 29, lines 17-26, though not represented in *MacLaren*'s "TRQ" they are nonetheless enqueued as claimed); if the read completion transaction entry is not present,

then determining whether a delayed/split transaction entry is present; and if the delayed/split transaction entry is present, then enqueuing delayed/split transaction entry into the transaction order queue (e.g., col. 29, lines 13-15).

Claim Rejections - 35 USC § 103

Claims 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacLaren in view of the widely known enhancement of the PCI standard, as evidenced by Willenborg (US 6477610).

Regarding claim 16, *MacLaren* discloses a plurality of registers being configured to receive a plurality of transaction entries as ordered by the first logic device (e.g., col. 28, lines 34-37); a second logic device adapted to receive the transaction entries from the plurality of registers and being programmed to select transaction entries according to PCI specifications (e.g., col. 26, lines 30-43); and a transaction order queue being configured to receive and enqueue the selected transaction entries (e.g., col. 29, lines 64-66).

MacLaren does not expressly mention the PCI-X bus; however Examiner takes Official Notice that this PCI enhancement specification is broadly known in the industry as exemplified by *Willenborg*. *Willenborg* discloses the PCI-X specification as the enhanced version of the PCI specification (e.g., col. 1, lines 54-61).

It would have been obvious to combine *MacLaren* with the PCI-X, because PCI-X is commonly known as an enhancement of the PCI standard. Therefore it would have been obvious, at the time the invention was made, for a person of ordinary skill in the art to combine *MacLaren* with an obvious standard enhancement.

Regarding claim 17, *MacLaren* also discloses the input source (e.g., col. 25, lines 55-56).

Regarding claim 18, *MacLaren* also discloses wherein the plurality of registers store the plurality of transaction entries received from the first logic device (e.g., col. 28, lines 34-37).

Regarding claim 19, *MacLaren* also discloses wherein the second logic device selects a single entry to send to the transaction order queue (e.g., col. 29, lines 64-66).

Regarding claim 20, *MacLaren* also discloses determining whether a posted write transaction entry is present; if the posted write transaction entry is present, then enqueuing the posted write transaction entry into the transaction order queue (e.g., col. 26, lines 60-63), if the posted write transaction entry is not present, then determining whether a read completion transaction entry is present; if the read completion transaction entry is present, then enqueuing the read completion transaction entry into the transaction order queue (e.g., col. 29, lines 17-26, though not represented in *MacLaren*'s "TRQ" they are nonetheless enqueued as claimed); if the read completion transaction entry is not present, then determining whether a delayed/split transaction entry is present; and if the

delayed/split transaction entry is present, then enqueuing delayed/split transaction entry into the transaction order queue (e.g., col. 29, lines 13-15).

Regarding claim 21, *MacLaren* also discloses wherein the transaction order queue enqueues one transaction entry per clock cycle (e.g., col. 30, lines 30-37).

Response to Arguments

Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be

calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H Knoll whose telephone number is 571-272-3636. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Khanh Dang
Primary Examiner

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